IN THE CLAIMS

1. **(Currently Amended)** A policy-based dynamic power management system for ~~dynamicaly managing power application to each of a plurality of devices in~~ a computer system, the computer system including a plurality of devices, wherein the power management system ~~comprising~~ comprises:

(a) a ~~flexible~~ clock generator circuit including at least one fixed rate clock signal oscillator, said generator circuit for generating ~~one or more~~ a plurality of clock ~~signals, wherein the frequency of each of said signals can be in a range from less than to greater than the frequency of said fixed rate clock signal; and~~ signals;

(b) a clock selector circuit ~~responsive to a rate of usage of each of said plurality of devices that directs a particular frequency of an output signal to be supplied~~ for providing a selected one or more of the plurality of clock signals to each of said plurality of ~~devices to maintain operation of each of said plurality of devices and minimize the total power being consumed by the computer system.~~ devices; and

(c) a clock policy unit for monitoring operational state of the computer system and for selecting the one or more clock signals based on factors including a current state of operation of the computer system and one or more programmable policies, wherein the policies indicate desired clock frequencies associated with the current state of operation.

2. **(Currently Amended)** The system of Claim 1 further comprising a static power management system for managing power application to each of said plurality of devices by withdrawing power from a device that is not currently active, and ~~re-applying power when said~~ applying power to the device when the device is needed to be active.

3. **(Currently Amended)** The system of Claim 2, wherein the static power management system includes a circuit for disconnecting ~~the address, and control data in and data out pins of a component of the computer system in order to reduce the power consumption of the computer system~~ certain pins of one or more of the plurality of devices.

4. **(Currently Amended)** The system of Claim 1, wherein the clock generator circuit includes a first oscillator that generates a first clock signal, a second clock oscillator that generates a second clock signal, and a programmable clock circuit that generates a third clock signal based on the second clock signal, wherein said clock ~~select~~ selector circuit selects one of the first, second and third clock signals ~~that is supplied to a portion of the computer system~~ to provide ~~that~~ a portion of the computer system with a ~~predetermined~~ desired clock signal.

5. **(Currently Amended)** The system of Claim 4, wherein the clock ~~select~~ selector circuit includes a ~~clock~~ state machine for ~~determining the clock state of the computer system at a predetermined time and a clock policy circuit for generating control signals to the clock select circuit in order to output the appropriate clock signal~~ monitoring the current operational state and selecting the one or more clock signals.

6. **(Currently Amended)** The system of Claim 5, wherein the ~~clock state machine provides~~ current operational state is selected from a group of states including an idle state when the computer system is waiting for an input, a busy state when the computer system is performing a task, a sleep state when the computer system has timed out due to inactivity and a dead state when power has failed to the computer system.

7. **(Currently Amended)** The system of Claim 6, wherein the clock ~~select~~ generator circuit includes a circuit that generates ~~a system clock~~ first and second system clocks, ~~a circuit that generates a processor clock and a circuit that generates a co-processor clock~~ wherein each of the clocks is independently and simultaneously operable.

8. **(Currently Amended)** The system of Claim ~~6, wherein,~~ 7, wherein the programmable clock circuit includes a phase locked loop, the computer system includes first and second processors and, during the idle state, the clock ~~select circuit generates no clock for~~ selector circuit:

disconnects clocks from the phase locked loop and ~~co-processor so that they are off, the clock select circuit generates the first clock signal for the processor so that the processor is clocked at a slow rate and the clock select circuit generates a high rate clock for an interrupt circuit so that the interrupt circuit is active and can increase the clock frequency for the computer system~~ the second processor;

and connects the first processor to the fist system clock.

9. **(Currently Amended)** The system of Claim ~~6~~ 7, wherein, during the busy state, the clock ~~select~~ selector circuit ~~generates a high rate clock signal for the processor, the co-processor and the interrupt circuits~~ connects clocks to the phase locked loop and the second processor and connects the first processor to the second system clock.

10. **(Currently Amended)** The system of Claim 6, wherein, during the sleep state, the clock ~~select~~ selector circuit ~~generates no clock signal for the processor and the co-processor~~ disconnects clocks from the first and second processors.

11. (Original) The system of Claim 5, wherein the clock state machine is controlled by an interrupt signal and software commands.

12. (Original) The system of Claim 4, wherein the programmable clock circuit generates a fourth clock signal.

13. (Original) The system of Claim 12, wherein the first, second, third and fourth clock signals have different frequencies.

14. (**Currently Amended**) The system of Claim 13, wherein the first clock signal frequency is 32 kHz, the second clock signal frequency is 24 ~~MhZ~~ MHz, the third clock signal frequency is 33 ~~MhZ~~ MHz and the fourth clock signal frequency is 66 ~~MhZ~~ MHz.

15. (Previously presented) The system of Claim 4 further comprising a time of day circuit that generates time of day clock signals based on the first clock signal.

16. (Previously presented) The system of Claim 4, wherein the clock select circuit includes means for dynamically changing the clock frequency applied to each device of the computer system based on the task being performed by the computer system.

17. (Previously presented) The system of Claim 4, wherein the clock select circuit includes a multiplexer.

18. (Previously presented) The system of Claim 4, wherein the programmable clock generator further includes a prescalar unit and a post scalar unit whose outputs are fed into a

phase locked loop that generates a third clock signal and a fourth clock signal having different frequencies.

19. **(Currently Amended)** A policy-based dynamic power management method for a computer system having a plurality of devices wherein ~~power is dynamically supplied to each device,~~ the power management method ~~comprising~~ comprises:

(a) generating ~~by a clock generator having a crystal oscillator one or more different~~ a plurality of clock signals wherein each ~~clock signal~~ of the plurality of clock signals has a different predetermined ~~frequency,~~ frequency; ~~and wherein said predetermined frequencies are selectable in a frequency range from less than to greater than a frequency of said crystal oscillator;~~ and

(b) supplying one or more of the plurality of clock signals to each of the plurality of devices, wherein the one or more clock signals are selected based on control signals received from a clock policy unit;

(c) ~~(b) dynamically~~ adjusting the frequency of the one or more clock signals ~~supplied to each device of the computer system in order to reduce the total power being consumed by the computer system.~~ responsive to changes in the control signals, wherein the clock policy unit configures the control signals based on factors including a current state of operation of the computer system and one or more programmable policies, wherein the policies indicate desired clock frequencies associated with the current state of operation.

20. **(Currently Amended)** The method of Claim 19 further comprising withdrawing power from certain devices ~~that are not currently active~~ to reduce ~~the~~ power consumption of the computer system ~~so as to provide static power management~~.

21. **(Currently Amended)** The method of Claim 20, wherein said withdrawing power includes disconnecting ~~the an address, and~~ address, control and data in and data out pins of ~~a device~~ one or more of the plurality of devices ~~of the computer system in order to reduce the power consumption of the computer system~~.

22. **(Currently Amended)** The method of Claim 19, wherein said generating further includes generating a first clock signal with a first oscillator, generating a second clock signal using a second oscillator, generating a third clock signal based on the second clock signals, and selecting by a programmable clock select circuit one of the first, second and third clock signals ~~that is supplied to~~ to supply a portion of the computer system ~~to provide that portion of the computer system with a predetermined clock signal~~.

23. **(Currently Amended)** The method of Claim 22, wherein said selecting further includes determining by a state machine the clock state of the computer system at a predetermined time and generating control signals to the clock select circuit in order to ~~output the appropriate~~ select a corresponding clock signal.

24. (Previously presented) The method of Claim 23, wherein said selecting further includes an idle state wherein the computer system is waiting for an input, a busy state wherein the computer system is performing a task, a sleep state wherein the computer system has timed out due to inactivity and a dead state wherein power has failed to the computer system.

25. (Previously presented) The method of Claim 24, wherein said selecting further includes generating a system clock, generating a processor clock and generating a co-processor clock wherein each of the clocks is independently and simultaneously operable.

26. (Previously presented) The method of Claim 24, wherein during the idle state, no clock signal is provided to the phase locked loop and co-processor so that they are off, and generating the first clock signal for the processor so that the processor is clocked at a slow rate and generating a high rate clock for an interrupt circuit so that the interrupt circuit is active and can increase the clock frequency for the computer system.

27. (Previously presented) The method of Claim 24, wherein during the busy state, a high rate clock signal is applied to the processor, the co-processor and the interrupt circuits.

28. (Previously presented) The method of Claim 24, wherein during the sleep state, no clock signal is applied to the processor and the co-processor.

29. (Original) The method of Claim 23, wherein the clock state machine is controlled by an interrupt signal and software commands.

30. (Original) The method of Claim 22 further comprising generating a fourth clock signal.

31. (Original) The method of Claim 30, wherein the first, second, third and fourth clock signals have different frequencies.

32. **(Currently Amended)** The method of Claim 31, wherein the first clock signal frequency is 32 kHz, the second clock signal frequency is 24 ~~MhZ~~ MHz, the third clock signal frequency is 33 ~~MhZ~~ MHz and the fourth clock signal frequency is 66 ~~MhZ~~ MHz.

33. (Previously presented) The method of Claim 22 further comprising generating time of day clock signals based on the first clock signal.

34. (Previously presented) The method of Claim 22, wherein the clock select circuit further includes means for dynamically changing the clock frequency applied to each device of the computer system based on the task being performed by the computer system.

35. (Previously presented) The method of Claim 22, wherein the clock select circuit includes a multiplexer.

36. (Previously presented) The method of Claim 22, wherein the programmable clock circuit further includes a prescalar unit and a post scalar unit having outputs that are fed into a phase locked loop that generates a third clock signal and a fourth clock signal having different frequencies.

37. **(Currently Amended)** A flexible clock generator, comprising:

a first oscillator that generates a first clock signal;

a second clock oscillator that generates a second clock signal;

a programmable clock circuit that generates a third clock signal based on the second clock signal wherein a frequency of said third clock signal can be in a range from less than to greater than a frequency of said second clock signal; and

a clock select circuit that selects one of the first, second and third clock signals that is supplied to a portion of the computer system to provide that portion of the computer system with a predetermined clock ~~signal.~~ signal, wherein the clock select circuit selects clock signals based on factors including a current state of operation of the computer system and one or more programmable policies, wherein the policies indicate desired clock frequencies associated with the current state of operation.

38. (Previously presented) The generator of Claim 37, wherein the clock select circuit includes a clock state machine for determining the clock state of the computer system at a predetermined time and a clock policy circuit for generating control signals to the clock select circuit in order to output the appropriate clock signal.

39. (Previously presented) The generator of Claim 38, wherein the clock state machine provides an idle state wherein the computer system is waiting for an input, a busy state wherein the computer system is performing a task, a sleep state wherein the computer system has timed out due to inactivity and a dead state wherein power has failed to the computer system.

40. (Previously presented) The generator of Claim 39, wherein the clock select circuit further includes a circuit that generates a system clock, a circuit that generates a processor clock and a circuit that generates a co-processor clock wherein each of the clocks is independently and simultaneously operable.

41. **(Currently Amended)** The generator of Claim 39, wherein, during the idle state, the clock select circuit ~~generates no clock for the~~ disconnects clocks from the phase locked loop and co-processor ~~so that they are off~~, the clock select circuit generates the first clock signal for

the processor so that the processor is clocked at a slow rate and the clock select circuit generates a high rate clock for an interrupt circuit so that the interrupt circuit is active and can increase the clock frequency for the computer system.

42. (Original) The generator of Claim 39, wherein, during the busy state, the clock select circuit generates a high rate clock signal for the processor, the co-processor and the interrupt circuits.

43. (Original) The generator of Claim 39, wherein, during the sleep state, the clock select circuit generates no clock signal for the processor and the co-processor.

44. (Original) The generator of Claim 38, wherein the clock state machine is controlled by an interrupt signal and software commands.

45. (Original) The generator of Claim 37, wherein the programmable clock circuit generates a fourth clock signal.

46. (Original) The generator of Claim 45, wherein the first, second, third and fourth clock signals have different frequencies.

47. **(Currently Amended)** The generator of Claim 46, wherein a frequency of the first clock signal is 32 kHz, a frequency of the second clock signal is 24 ~~MhZ~~ MHz, a frequency of the third clock signal is 33 ~~MhZ~~ MHz and a frequency of the fourth clock signal is 66 ~~MhZ~~ MHz.

48. (Previously presented) The generator of Claim 37 further comprising a time of day circuit that generates time of day clock signals based on the first clock signal.

49. (Previously presented) The generator of Claim 37, wherein the clock select circuit includes means for dynamically changing the clock frequency applied to each component of the computer system based on a task being performed by the computer system.

50. (Previously presented) The generator of Claim 37, wherein the clock select circuit includes a multiplexer.

51. (Previously presented) The generator of Claim 37, wherein the programmable clock generator includes a prescalar unit and a post scalar unit whose outputs are fed into a phase locked loop that generates a third clock signal and a fourth clock signal having different frequencies.

52. (**Currently Amended**) A power management method for a computer system comprising:

dynamically managing power application to each of a plurality of devices of said computer system including

a) first sensing a current operational usage of said each ~~said~~ device; ~~and~~

b) adjusting a frequency of a clock signal from a clock generator to said each ~~said~~ device, said frequency in proportion to said usage, wherein said clock signal is supplied by a flexible clock generator including at least one oscillator, and wherein said generator ~~can output~~

provides at least one signal having a frequency adjustable from less than to greater than a frequency of said at least one ~~oscillator.~~ oscillator; and

c) responsive to interrupt and software command, modifying current operational usage of one or more of said each device.

53. **(Currently Amended)** The method of Claim 52, further comprising:

statically managing power application to said each ~~said~~ device including

a) second sensing to determine if a system device is being used;

b) withdrawing power including a clock signal from a device, if said device is not being used;

c) determining if an unpowered device is needed; and

d) applying power including a clock signal to said unpowered device if said device is needed.

54. **(Currently Amended)** The method of Claim 53 further comprising:

optimizing by a device controller to manage said dynamic power application to said each device for a lowest computer system power consumption consistent with required operation of said each ~~said~~ device.

55. (Previously presented) The method of Claim 53 wherein said withdrawing power includes gating off logic and a clock signal to a device, and applying power includes reapplying logic and a clock signal to said device.